An Analysis on Spin Wave Logic and CMOS Interface

Qian Wang

Department of Electrical Engineering

University of California, Los Angeles

Email: qianwang@ucla.edu

Advisor: Dejan Marković

Abstract

Spin wave devices can be used to build generic logic functions. Their low-power property offers competitive potential in future applications. In this project, ideas of implementing Spin Wave Logic are discussed. It is seen that low-power logic structure is possible and CMOS interface circuit is available if the size of single Spin Wave Logic block is limited by practical concerns (e.g. routing congestion).

Chapter 1

Introduction

Over the past several decades, aggressive scaling of complementary metal-oxide-semiconductor (CMOS) technology gave rise to an exponential growth of semiconductor industry. However, in recent years, many short channel effects emerged as the feature size of CMOS devices approached nanometer level. For example, increasing device leakage has impaired and will stop energy efficiency improvement through CMOS scaling. These problems force researchers to consider alternative options (including material, device and logic paradigm) to bypass the energy brick wall for CMOS.

Spin-based devices are popular candidates since computations are no longer executed through charge transfer driven by electrical field as in CMOS. Instead, they consume much less power because only electron spin orientation has to be switched during the computation and no physical movement of electron is involved.

1.1 Spin Wave Logic

In this project, we mainly discuss a specific implementation of spin-based devices called Spin Wave Logic. Spin wave is a collective oscillation of spins around the direction of magnetization propagating in a
wave-like manner in the ordering magnetic materials. Wave as it is, it holds interference property during propagation and thus can be used to perform logic operation.

Spin Wave Logic mainly consists of magneto-electric cells (ME Cell) connected via spin wave buses (Bus). ME Cell, as shown in Fig. 1, has a sandwich-like structure including from the bottom to top a layer of conducting magnetostrictive material (e.g. Ni, CoFe), a layer of piezoelectric (e.g. PZT), and a metallic contact (e.g. Al). This structure serves as a parallel capacitor providing interaction between electric signals in top layer and magnetization in bottom layer. Input data can be received by ME Cell at metallic contact in form of positive or negative electrical pulses (predicted ±10mV). These pulses result in different magnetic polarization rotation within ME Cell, thus two different kinds of spin waves, which have 180° phase difference, may be excited into the Bus. In this way, bit information is passed from positive or negative electrical pulses to phase of spin wave in the Bus. Alternatively, input data can also be received through incoming spin waves. When a spin wave approaches ME Cell through the Bus and at the same time an electrical pulse is present at the metallic contact, internal magnetization of ME Cell will be written correspondingly by the phase of incoming wave, and a new wave is released into downstream Bus. The existence of pulse is critical here since without the energy it provides, the strength of incoming spin wave is insufficient to flip the destination ME Cell.

![Magneto-electric cell](image)

Figure 1: Structure of ME Cell (Courtesy of A. Khitun)

Logic operation is conducted in spin wave buses in the form of wave interference. The Bus is a ferromagnetic film (e.g. NiFe) for spin wave to propagate along. Reference [1] shows that spin wave within Bus has a typical group velocity around $10^4$m/s, coherence length more than 10μm at room temperature. Thus interference property of spin wave is guaranteed. Therefore, two travelling spin waves with same phase (i.e. same bit information) would interfere constructively, while those with 180° phase difference would interfere destructively. The phase of resultant spin wave hence denotes bit output of the operation.
1.2 Motivation for CMOS Interface

By cascading stages of ME Cells and Buses, realizing complicated logic seems straightforward. However, there are some differences between Spin Wave Logic design and CMOS VLSI design. Firstly, in CMOS charge transfers through metal strip wires. The lengths and shapes of these wires are flexible as long as they can pass design rule check. But for Spin Wave Logic, Bus length is a critical parameter with respect to circuit function, so it cannot be adjusted arbitrarily. Secondly, Bus has to be straight so that reflection at corners can be suppressed. Thirdly, there are multiple routing layers available in modern CMOS design, but the availability of multi-layer is not demonstrated yet in Spin Wave Logic.

Considering these routing disadvantages in Spin Wave Logic design, problems may exist in large scale integration later when it is applied. Thus, a study on possible CMOS interface is necessary. In this way, a large Spin Wave Logic computation block can be divided into smaller ones and have their outputs read by connecting CMOS circuitry.

1.3 Overview of Previous Work

In 2002, Covington et al. presented temporal simulation and experiment of spin wave propagation in ferromagnetic films [1]. Since then, effort has been put into utilizing spin wave to process information [2]-[4]. For example, spin wave is applied in image processing tasks [4]. There ME cells are deployed in 2D arrays with Bus connections to ensure information exchange among neighboring cells. Then, image processing functions like low-pass filtering or edge detection can be performed.

A more ambitious idea is to build generic digital logic out of Spin Wave devices. There are a few articles conceptually discussing the possibility to apply Spin Wave devices in logic circuits [5], [6] but circuit level analysis and comparison against CMOS is only found in [7]. This report presents a method to implement 1-bit and 2-bit adders, but it requires some ME Cells to generate spin waves with amplitude exactly twice as large as those from other ME Cells. In this project, other possibilities are explored and practical considerations before large scale circuit application of Spin Wave Logic are covered, in order to provide some guidelines for applications.

1.4 Project Outline

In subsequent chapters, a study on several aspects of implementing Spin Wave Logic is presented. Chapter 2 discusses methods and limitations of building Spin Wave Logic blocks, and a comparison against CMOS is made. Chapter 3 provides possible CMOS circuits for information read-out at output ME Cells. Chapter 4 summarizes and discusses future work.
Chapter 2

Spin Wave Logic Gates

In Chapter 1, operation principle of Spin Wave Logic is described. With this knowledge, we can combine multiple ME Cells and Bus to implement specific logic gates, including some of the most basic combinational and sequential logic blocks. Estimation on performance comparison against their CMOS counterparts is shown to demonstrate Spin Wave Logic’s potential advantages.

2.1 Combinational Logic

Starting with ME Cell and Bus, the simplest logic functions are Buffer gate and Not gate. A Buffer can be built with 2 ME Cells and connecting Bus with length $n\lambda$, as shown in Fig. 2. In this way bit information is passed intact from input cell to output cell. On the other hand, Not gate requires inverted bit information at output cell, so connecting Bus should have length $(n + 0.5)\lambda$, as shown in Fig. 2. Since the difference between Buffer Gate and Not Gate is merely Bus length, Bus must be fabricated with certain accuracy. A length offset of $0.25\lambda$ would make it impossible to tell the difference between bit 0 and bit 1. Therefore a safety offset should be smaller than that, for example $0.1\lambda$. Typically $\lambda$ ranges around 100nm, so $0.1\lambda$ is around 10nm. Nano fabrication at this accuracy level might be another challenge before this technology is applied in reality.

More complicated logic functions take the advantage of spin wave interference property. The basic building element is a 3-input Majority gate, shown in Fig. 3. Three wave signals travel through Buses of the same length $(n\lambda)$ and merge at output cell. In this way, waves generated by opposite bit information at input interfere destructively and cancel out each other. Thus, magnetization direction at output is the majority of three input states. Any of the three branches can also have length adjusted by $0.5\lambda$ so that
an additional inverter is embedded in that input. This results in several variants from the original Majority gate.

![MAJ gate](image)

Based on 3-input Majority gate, if one of the inputs is fixed at logic 1, it reduces to a 2-input OR gate. If one of the inputs is fixed at logic 0, it reduces to a 2-input AND gate. With AND, OR and Not gate, it is sufficient to build arbitrary combinational logic function. Since AND and OR gates are actually variants of 3-input Majority gate, building logic is simply factoring logic expression in the form of Majority gates. Here is a list of some logic functions.

\[
AB = MAJ(A, B, 0)
\]

\[
A + B = MAJ(A, B, 1)
\]

\[
A \oplus B = MAJ[MAJ(A, \bar{B}, 0), MAJ(\bar{A}, B, 0), 1]
\]

\[
ABC = MAJ[MAJ(A, B, 0), C, 0]
\]

\[
A + B + C = MAJ[MAJ(A, B, 1), C, 1]
\]

Different from traditional CMOS design, layout of Spin Wave Logic must be considered at very beginning of the design flow. For some simple functions, layout can be done by cascading Majority gates layout. However, layout may be difficult for complicated gates. 1-bit full adder can be taken as an example. Here inputs are operands \( A, B \) and input carry \( C_i \), outputs are sum \( S \) and output carry \( C_o \). Expressions of outputs in terms of inputs are:

\[
C_o = AB + AC_i + BC_i
\]
With majority gates, they become a two-stage chain with an intermediate ME Cell $I$:

$$C_o = MAJ(A, B, C_i)$$

$$I = MAJ(\overline{A}, B, C_i)$$

$$S = MAJ(A, \overline{C_o}, I)$$

Thus, a possible layout of 1-bit adder (compact structure) is shown below in Fig. 4. Bus lengths are carefully tuned so that they form the three required Majority gates.

Figure 4: A compact 1-bit Adder layout

With proper timing on top of the ME Cells, this structure offers the function of a 1-bit adder. But it also has high requirement on fabricating Buses with fixed lengths and angles. Size and shape of ME Cells also determine whether they can sit perfectly in the structure.

A more conservative plan is to have a Coplanar layout, as shown below in Fig. 5. This layout also offers the function of a 1-bit adder. Although area-wise it is not as compact (twice as large) and has more ME Cells, it is easier to fabricate by building majority gates in a straight line.
2.2 Sequential Logic

Sequential logic is relatively easy to implement. Each ME Cell acts as a non-volatile bit memory, so one single cell is able to play the role of a flip-flop. Considering that a flip-flop consists of many transistors in CMOS technology, using Spin Wave Logic is extremely beneficial in sequential designs.

Since flip-flop overhead is largely mitigated in Spin Wave Logic, dividing a complicated combinatorial logic function into multi-stage pipeline structure becomes attracting. Here a 2x2 Multiplier is taken as an example. Inputs are \{A_1, A_0\} and \{B_1, B_0\}, outputs are their product \{C_3, C_2, C_1, C_0\}. Logic relation between inputs and outputs is organized in Fig. 6.

According to previous section, AND and XOR gates shown in the figure can be built with Majority gates. Thus after a direct mapping from Fig. 6, Spin Wave Logic implementation can be described in a pipeline structure, shown in Fig. 7. ME Cells are labeled with different notations according to their
functions. Blue arrows indicate Bus connection between two ME Cells. The intersecting arrows mean that Buses have to run into each other. This is impossible before multiple layers of waveguide are available. Therefore this example demonstrates that a universal method for complicated logic layout is difficult given Spin Wave Logic development right now.

2.3 Comparing with CMOS Counterparts

In the following paragraphs, a performance comparison between logic functions built with CMOS and with Spin Wave Logic is presented. Sample functions are chosen to be Inverter, 2-input NAND gate, and 1-bit Adder (compact structure). Performances are characterized by delay, energy and area. For CMOS part, functions are implemented with 1V TSMC 65nm technology.

Estimation of Spin Wave Logic blocks is made in the following way. Delay between applied pulses and spin wave excitations is assumed to be 100ps [7]. Wave propagation delay is derived from Bus length and group velocity. By summing these along the critical path, delay estimation is achieved. Energy cost for spin wave excitation per cell is estimated as 4.8aJ [8]. This energy number comes from the energy barrier between two magnetic states and an assumed energy conversion efficiency of 10% [8]. Area estimation directly comes from layout diagram. Data for CMOS components are measured from TSMC 65nm models under FO-4 condition.
Table 1 Performance Comparison between Spin Wave Logic and CMOS Logic

<table>
<thead>
<tr>
<th></th>
<th>Delay (ps)</th>
<th>Energy (aJ)</th>
<th>Area (μm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Spin Wave</td>
<td>CMOS</td>
</tr>
<tr>
<td>Inverter</td>
<td>205</td>
<td>13</td>
<td>9.6</td>
</tr>
<tr>
<td>2-input NAND</td>
<td>210</td>
<td>14</td>
<td>19.2</td>
</tr>
<tr>
<td>1-bit Adder</td>
<td>335</td>
<td>76</td>
<td>28.8</td>
</tr>
</tbody>
</table>

From this comparison table, we can see that Spin Wave Logic mainly has its advantage at low energy consumption and low area cost while its operation speed is lower. Interestingly, when design complexity rises, Spin Wave Logic designs become more preferable compared to CMOS designs. For more complicated structures than 1-bit Adder, Spin Wave Logic has the potential to operate faster if pipeline structure is taken into account. Thus we can find that Spin Wave Logic will outperform CMOS designs if its fabrication and layout problems are all settled.

Chapter 3
CMOS Interface

The discussion above draws an outline for possible implementations of Spin Wave Logic blocks. However, increasing difficulties in large scale layout are likely to limit the available size of Spin Wave Logic blocks. Hence exploring CMOS circuitry to read out bit information at output ME Cells is meaningful. In this chapter, interface circuit is built to capture bit information and represent it in CMOS voltage level. The energy cost for each read is estimated, denoting the optimal number of ME Cells assigned to one read-out port.

3.1 Modeling output ME Cell

The first step of interface design is to model the output Cell in a CMOS-compatible form. Because the fabrication of ME Cells is still in an elementary stage, an explicit model is not yet available. Right now, circuit work is based on two possible suggestions.

One of them is proposed by Khitun [8]. In his article, output ME Cells are described to induce ±10mV level voltage signal between metallic contact and ground. This phenomenon is experimentally verified by Sekiguchi et al. [9] and the voltage waveform has a wave packet shape. Seeing from CMOS side, output impedance can be modeled as a resistor in parallel with a capacitor, where \( R_{\text{out}} \approx 100kΩ \) and \( C_{\text{out}} \approx 1fF \), as shown in the figure below. With this information, we can proceed with CMOS circuit design in the following section.
The other suggestion is proposed by Alzate [10]. In his opinion, output elements can be implemented with Magnetic Tunnel Junction (MTJ). The operation of an MTJ as Spin Wave Logic output cell is similar to an output ME Cell, except that bit information presents in the form of variable MTJ resistance instead of induced voltage. Incoming spin wave signal writes to the magnetization direction of free layer of MTJ with the help of a triggering pulse across the MTJ. After that, resistance of MTJ will be one of two possible values $R_p$ or $R_{AP}$. Then CMOS circuit simply needs to sense the resistance to discern bit information. Circuit model for the MTJ is shown below, similarly a resistor in parallel with a capacitor. Here parameter values are $R_p = 50\, k\Omega$, $R_{AP} = 75\, k\Omega$, $C_{out} \approx 1\, fF$, largest allowed current $I_{safety} = 100\, \mu A$.

3.2 Reading with Voltage Sense Amplifier

Both methods of modeling require a circuit to sense relatively small voltage difference and amplify that to CMOS storage level (around 1V). Thus a sense amplifier can be used as read-out circuit for both suggestions described in the previous section. Circuit simulation is performed with TSMC 65nm technology and energy cost of reading is speculated.

3.2.1 Sense Amplifier with Offset Cancellation Loop

In Khitun’s suggestion [8], sense amplifier needs to detect 10mV level voltage difference. In modern CMOS technologies, mismatch between regular sized transistors is so large that input-referred offset of the comparator grows more than 10mV. Thus the comparator is unable to make a correct reading based on 10mV input difference comparing to reference voltage. Increasing the sizes of input transistors pair
helps alleviating the problem [11], but higher energy cost associated with up-sized transistors makes it difficult to maintain energy benefit of Spin Wave Logic. Conventionally, pre-amplifiers are used to reduce input offset [12], but the high performance amplifier is also power-hungry.

A practical idea to overcome the problem is using a comparator with low-power feedback loop to calibrate the input transistors. [13] The circuit is shown below.

---

**Figure 10: Calibration Feedback Loop and Charge Pump (Courtesy of M. Miyahara)**

---

**Figure 11: Comparator Schematic (Courtesy of M. Miyahara)**
In calibration phase, same DC inputs are fed to the comparator and comparator outputs $CMP_{out-}$ and $CMP_{out+}$ adjust the charge on capacitor $C_H$ until it comes to a stable state when $CMP_{out+}$ oscillates between 0 and 1 in each clock cycle. Then it is safe to say the comparator is calibrated.

After that, comparator can be switched to evaluation phase. Now induced voltage coupled with common mode voltage 0.5V is fed to one input and 0.5V alone is fed to the other input. Voltage difference is sensed and amplified to full swing level at comparator outputs.

Simulation result also shows that input-referred offset voltage has a standard deviation less than 2mV, making it safe to trust bit reading result from 10mV difference. Initial calibration takes 60nS to complete while reading in evaluation phase takes 115pS. For each reading, the comparator consumes about 6.5fJ energy.

3.2.2 Cross-Inverter based Sense Amplifier

In Alzate’s suggestion [10], MTJ is used as output element. Variable resistance can be sensed by a cross-inverter based sense amplifier, [14] as shown below. $R_{ref}$ is a reference resistance with value $\frac{R_{AP}+R_P}{2}$. Calibration loop is not need here since high resistance of the MTJ guarantees a high voltage difference between MTJ and $R_{ref}$ when they have similar current flowing through.

Simulation result shows that reading delay is 100pS and reading energy is 6.4fJ.

In conclusion, the two suggestions result in different circuit topologies, but energy costs for reading are approximately the same at 6.5fJ. Since this is over 1000 times larger than 4.8aJ, the estimated energy cost for one ME Cell per operation, one output port must be assigned to large scale integration with thousands of ME Cells to maintain energy efficiency in tens of aJ.
Chapter 4

Conclusion

In summary, this work discusses possible methods and practical considerations in building generic digital logic with Spin Wave Logic concept. It also includes comparison against CMOS logic blocks and possible CMOS circuitry to read out Spin Wave Logic output signals. However, large scale layout needs to be done with the help of multiple Bus layers. If this is done, comparison results show that Spin Wave Logic has the potential to be highly energy and area efficient with comparable loss on circuit delay compared with CMOS gates. CMOS read-out circuit is also discussed. Simulation results demonstrate that communicating with CMOS circuit is energy efficient only when an I/O port is shared by a large number (greater than about 100) of ME Cells.

References


